Microprocessor

There are two way for Binary Addition
1) Normal Binary Addition
2) BCD Addition (Binary Coded Decimal No)

1) Normal Binary Addition

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2) BCD Addition :- These BCD start from 0 and end with 9. They donot have any base

Number System
1) Decimal → 10
2) Binary → 2
3) Octal → 8
4) Hexa decimal → 16

- All of the instruction in Microprocessor written with hexadecimal no.
- Most of the System relates binary no from any types of no because binary no can easily be converted in octal no as well as hexadecimal

$(100.973)_{10}$

2 | 100		.973
2 | 50 – 0		× 2
2 | 25 – 0		1.946
2 | 12 – 1		× 2
2 | 6 – 0		1.892
2 | 3 – 0		× 2
1 – 1		1.784

$(1100100.111)_2$

8 | 100		.973
8 | 12 – 4		× 8
1 – 4		7.784
		× 8
		6.272

$(114.76)_8$

16 | 100		.973
6 – 4		× 16
		5.858

$(64.5D)_{16}$

→ 100+973

0001 0000 0000
+ 0001 0111 0011
1010 0111 0011
0110
1000 0111 0011
1073

Generated by CamScanner from intsig.com

Rules :- 1) When result of two no after normal binary addition is greater than 9 then 6 will added

2) If Result of two no less than 9 and carry will generate then 6 will be added.

3) If result of two no less than or equal to 9 and carry will generate result will be same

577+489

577 0101 0111 0111

489 0100 1000 1001

1010 0000 0000

0110 0110 0110

10000 0110 0110

1066

→ Substraction :- In 2 way Substraction can be done

1) Normal Binary Substraction

Input		output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

2) 1's complement Substraction : Also known as inversion

45-15

45 → 101101

15 → 001101

32 16 8 4 2 1

101101

001111 → 15

101101

110000

1 01 1,10 1

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2	30
2	15 – 0
2	7 – 1
2	3 – 1
2	1 – 1
	0 – 1

32 16 8 4 2 1
0 1 1 1 1 0

10111101
+1
11011110

9's Complement

64 32 16 8 4 2 1

BCD Substraction → 9's & 10's Complements are used in BCD Substraction.

Microprocessor :- 8085 is the most popular microprocessor in 8 bit series because it is fastest microprocessor because of NMOS Technology (N-channel Metal Oxide Semiconductor). In NMOS Current Conduction is only due to electronics. 8 bit microprocessor means 8 bit data can be executed at a time. For more than 8 bit first function related with first 8 bit after execution of first 8 bit another 8 will be executed means time level increase for more than 8 bit executed because therefore of the region it operate at frequency of 3.07 megaHz

Another advantages is that it operate at

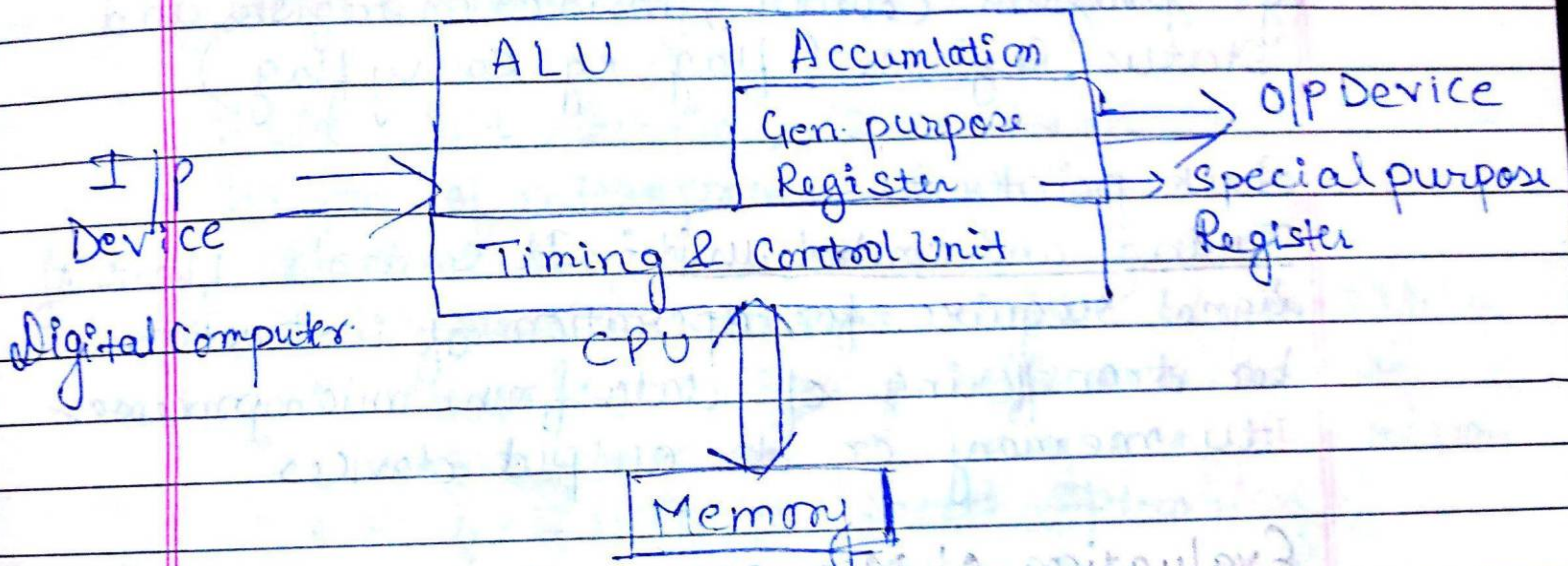
power supply of +5V

→ One more advantage of 8085 it is compatible with TTL logical family

→ It is 40 pin Ic package Earlier Microprocessor intel 8080 were primost technology because of this 8080 is not studied.

→ One more disadvantage is that it requires 3 power supply for its operation and it is not compatible with TTL Technology

General Architecture of 8085:



ALU stands for Airthematic and Logical Unit All Airthematic operation eg substraction, addition and logical operations are performed using ALU apart from these ALU also perform rotation, shifting, clearing and Refreshing

Accumlator: It is the primary register of 8085 all the operation performed by ALU gives result that result is stored in Accumulator and also operation are performe

using Accumlator

→ General purpose Register :- 8085 having 6 general purpose register. Each of 8 bit long (B C D E H L)
It is used for Temporary storage during execution of instruction

→ Special purpose Register :- The Register are used by Microprocessor itself. User cannot use these Register
eg :- program Counter, instruction register and Status Register (flag eg carry flag)

Stack pointer :-
Timing and Control unit :- It controls flows of signal require for operation of instruction for transffering of data from microprocessor to memory or to output devices

Evaluation of Microprocessor :-
Intel 4004 was first microprocessor based upon premost technology. It was of 4 bit processing speed was very slow than 8 bit microprocessor was again dereloped by in 8080 & 8085, 8080 was PMOS and 8085 is on N-MOS
Intel then introduce 16 bit microprocessor 8086, 8088 and 80186 there 16 bit micro processor were very fast because of VLSI Technology

VLSI uses C-MOS logic family (complimentary metal Oxide semiconductor)
In this technology for designing any logic ckt there is need of Resister

Registors are passive elements and register design by active element. If resister will not be used in the circuit having affect will be zero.
Then Intel introduce 32 bit microprocessor intel 80386, 80486, pentium 1,2,3,4 after that 64 bit system was developed.

8 bit, 16 bit, 24 bit, 32 bit, 64 bit defines word length of microprocessor.
8 bit = 1 byte
32 bit mean microprocessor will perform 32 bit data at a time, speed will increase by increasing word length because of this reason clock frequency or speed operation of microprocessor for different bit.

Intel	Year	Speed of operation	Bitwise	Memory
4004	1971	750 K Hertz	4 bit	1 Kilobyte
8085	1976	3.07 Megallz	8 bit	64 Kb
8086	1982	5-10 MHz	16 bit	1 Megabyte
80286, 80386	1985	6-12 MHz, 20-33 MHz	16 bit	16 Mb
80486	1989	25-100 MHz	32 bit	4 gigabyte
pentium 1	1993	60-200 MHz	32 bit	4 gb
pentium 2	1997	230-400 MHz	32 bit	4-6 GB
pentium 3, 4	2000	upto 1.3 gHz, upto 1.3-1.5 gHz	32 bit	4-6 GB
Itanium	2001	upto 3 GHz	64 bit	4-12 GB

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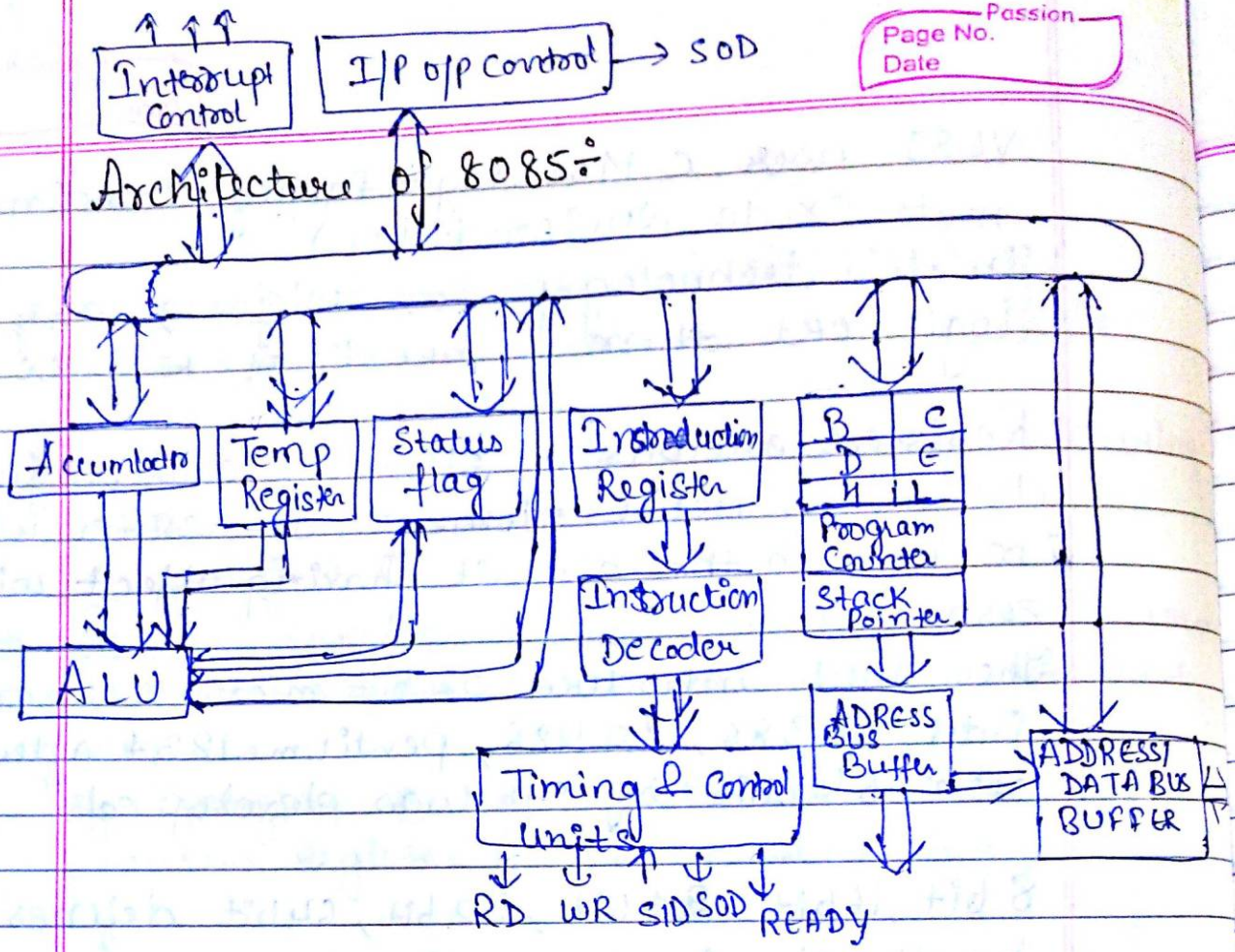
Architecture of 8085:-



Registers:-

1. Simple register (main register)
2. General purpose register
3. Special function register
4. Other Register

Simple register/

1. Accumlator + ① 8 bit
   ② Used as a register for storing one data when two are arithematically and logically operated
   ③ After ALU operation result is also stored in accumlator
   4) When single no is to be logically operated only accumlator is used as a storage as well as storing result after execution

(2) General purpose register :- B, C, D, E, H & L are used as General purpose register

(2) Each 8 bit long

(3) Pairing can also be done in a standarded way to stored 16 bit data
eg (B-C, D-E, H-L)

4) H-L pair is an exceptional pair which is used as a memory pointer to locate an address
LXI (H), 2000H

H recognise H-L pair of general purpose register

Load 16 bit data immediately in H-L pair. It mean 2000H is the location of memory where data is stored and it is recall by an instruction MOV A, (M)

M locates memory location 2000H which is pointed by H-L pair

Exceptional point in 8085 microprocessor 16 bit additional can only be possible by using an instruction DAD

(3) Special function registers :- Stack pointer & program Counter are two special function register
These are those register which are used only by microprocessor not by user.

Program Counter :- It is a 16 bit register
(2) Used by microprocessor
(3) It holds the address of next instruction to be executed for eg:- After execution MOV A, instruction program Counter will be automatically incremented and points next location of memory where another data is stored

Stack pointer :- It is used when interrupt is generated by microprocessor. Interrupt is a command which stop the main program for a moment at that time program Counter location will be stored in a stack and program Counter will be loaded with a new address through which Sub routine is called

Sub-routine is a small program which is used many times by main program. For eg generating delay in main program after execution of each instruction.

Stack :- Small memory location acquired by main program in RAM area.

4) Others Register :- 1) Instruction register
2) Temporary register.

1) Instruction Register) 8 bit long
2) Will stored opcode (8 bit) of an instruction.

2) Temporary Register :- 1) 8 bit long
(2) Will store data temporarily before execution of instruction

(2) Instruction Decoder :- Bits is generated by instruction register will be decoded by instruction decoder, it mean digital signal will be converted in analog signal and these signal will be sent to timing & control unit

Timing & Control Unit :-
Signal generated by ID will be provided by microprocessor by a controlled way using this unit eg :- RD, WR, SID, SOD

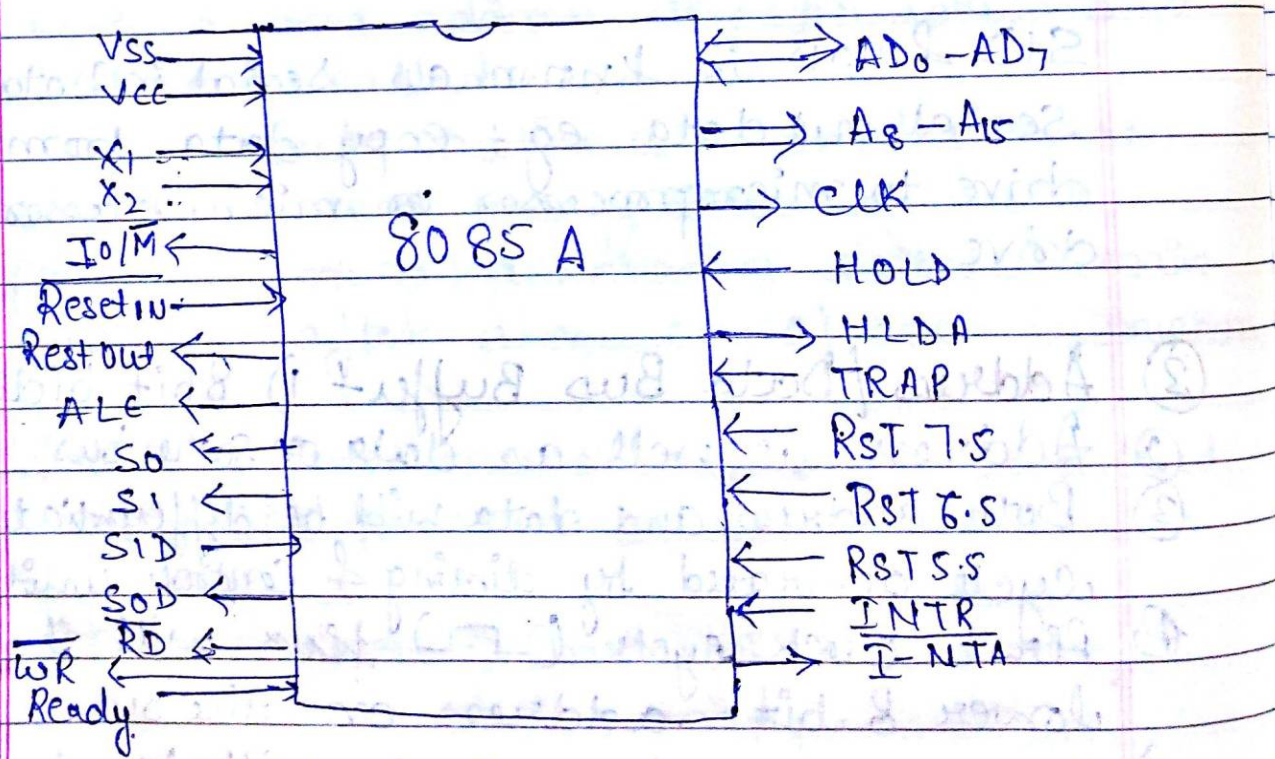
SID & SOD is known as serial in Data and serial out data eg :- copy data from pen drive to microprocessor or microprocessor to pen drive

(3) Address / Data Bus Buffer :- 1) 8 bit bidirectional
(2) Address as well as data on same bus
(3) Both address and data will be differentiate by clock cycle generated by timing & control unit
(4) First clock cycle (_⌐¬_) first will load lower 8 bit address on the bus
(5) Two more clock cycle will load data on address bus.
$AD_0 - AD_7$

4) Address BUS Buffer :- $A_8 - A_{15}$ Higher order address bus unidirectional. Address Latch - 74373 will be used as a temporary storage (latch) for lower bit of address. If address will high then address is high. or vice versa.

8085 AH1 is only microprocessor which operates at 6 MHz because of H-MOS technology.

Pin Diagram of 8085 :- 40 pin IC package with DIP technology
↳ Dual inline



1) $AD_0 - AD_7$:- Address bus bidirectional. In this bus lower 8 bit address as well as the data is transfer depending upon timings given by control unit using address latch.

during first clock cycle lower 8 bit address is transfer and two more clock cycle will be required to transfer 8 data on the same bus. when address is transfer it lower 8 bit be stored in temporary register

2) $A_8 - A_{15}$:- This bus carry higher 8 bit address which will be present for all three cycle when lower 8 bit address as well as data is sending in bidirectional bus then 16 bit address will be store and 8 bit data is transfered This technique is known as time multiplexing technique because it depend upon time sharing of address and data on bus.

3) Clock :- This pin generates clock frequency of 3.07 mHz and will be applied to other digital IC's which require same clock pulse

4) TRAP (RST 7.5, RST 6.5, RST 5.5) :- These pins are known as interrupt and also define as hardware interrupt because these are generated through microprocessor. These interrupt are initalise on the basis of priorities

Trap
RST 7.5
RST 6.5
RST 5.5

Priority in descending order ↓

Interrupts can also be differentiated on the basis of there processing and are known as maskable and non maskable interrupts

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TRAP → Non maskable interrupt

RST 7.5
RST 6.5
RST 5.5
→ Maskable interrupt

Maskable interrupt ÷ There processing can be stop at anytime. Trap exceptional interrupt because if executed cannever be disable

→ INTR ÷ Also known as hardware interrupt, processing little bet different. Amongst all interrupt this interrupt have lower priority when this Interrupt activated Program Counter does not increase its Content

→ $\overline{\text{I-NTA}}$ ÷ Interrupt Acknowledge Symbol. Bar defined as active low signal if Zero will apply to this pin $\overline{\text{I-NTA}}$ will activated mean acknowledge signal is generated only interrupt request signal is recieved by microprocessor.

→ Vss ÷ Ground Signal.

→ Vcc ÷ power supply +5V

→ X_1 & X_2 ÷ These pins are used for generation of clock frequency of 6MHz. Between these two pins

Circuit without any input generate oscillation it work only when output voltage is in phase with input voltage. when output applied to

Input known as positive feedback network

Frequency divider network is required to divide frequency from 6 to 3MHz

→ IO/$\overline{M}$: This pin is used to define whether address is of memory or input output device. If this pin is low address is of memory.

IN OIH : At this time input output (IO/$\overline{M}$) pin will be high. i.e IO/$\overline{M}$ = 1

→ $\overline{\text{RESET/IN}}$: Active low signal, this pin when low used to reset the system

→ RESET/OUT : when high show system has be reset

→ ALE (Address Latch Enable) : when high lower bit address is transferred on the bus and when low data is transferred only using IC 7437

→ S_0 & S_1 : Known as status signal used to define instruction operation

S_1	S_0	operation
0	0	opcode fetch operation
0	1	Write operation
1	0	Read operation
1	1	Halt operation (stop)

→ SID (serial in Data) & SOD (serial out Data):
These two pin are use for serial operation for example copy data from pen drive to computer or computer to pendrive.

→ $\overline{RD}$: Read operation, Active low, data is easily recognise from memory if $\overline{RD} = 0$

→ $\overline{WR}$: When any operation is performed on memory for eg moving content from accumulator to memory.

→ READY : When active high show that peripheral device is high for transfering of data.

→ HOLD signal : This signal when activated shows that when any other device is requesting for address and data bus, when activated it release the use of these buses.

→ HLDA & Hold request is recieved by microprocessor

→ Instruction of 8085 :
Instruction is a command given by computer to perform specific operation.
8085 microprocessor having 80 instruction sets Each microprocessor of different company having different instruction set. And these instruction set are not compatible with each other for eg intel & motorola microprocessor having their diffrent instruction set.

These are divided into different group.

1) Data transfer group
2) Airthematic Group
3) Logical Group.
4) Branch Control Group.
5) Input output & machine Control Group.

1) Data transfer group: Instruction related with transfering, loading, storing and some exceptional instruction related with stack pointer comes under this group for eg MOV, STA, LDA, STHL etc.

2) Airthematic Group: Instructions related with Airthematical operation comes under this group. for eg ADD, SUB, increment & decrement.

3) Logical group: Instruction related with logical operation for eg OR, EXOR, AND, Complement etc
Resetting can also be done using logical operation.

4) Branch control Group: Instruction related with Conditional operation comes under this group for eg jump, instruction related with sub routine (CALL & return) and restart instructions (instruction related with Software interrupts

5) Input output & machine Control Group: All instruction are related with Input & output

Ports as well as controlling of machine is also perform or comes under this group. eg IN, OUT, instruction related with enabling and disabling of Interrupt and also Halt operation comes under this group.

Addressing modes of 8085 :- 5 modes comes under this category

1) Direct Addressing mode.
2) Register Addressing mode
3) Indirect Addressing mode
4) Immediate Addressing mode
5) Implict Addressing mode

Addressing mode :- These are define as the way of data transferring between register either having direct address or indirect address

(2) Data transferring within the register either direct or indirect

(3) Operation on data either self operation means single register will be used for whole of the operation or with the help of another register.

1) Direct Addressing mode :- Address is given in the given instruction for eg :- LDA 16 bit Address. Load Directly the contents given by 16 bit address in instruction to accumulator

2) Register Addressing mode :- This instruction copy the content of B register to accumulator
MOV A, B

3) Indirect Addressing mode: LXI H,2000H
MOV A,M

LXI H,2000H → This instruction will load 16 bit data in HL pair immediately. Now HL pair will act as a memory pointer which locate memory location in RAM area given by 2000H

MOV A,M: It will copy the content of memory specified by HL pointer into accumulator.

4) Immediate Addressing mode: Data is directly given in the instruction for eg MVI A,(30H) → 8 bit data. 8 bit data is immediately copied into Accumulator

5) Implicit Addressing mode: If Data operation is performed by itself (with the help of Accumulator) then known as implicit accumulator

Accumulator is only register which stores result.
for 16 bit operation HL register will be used

Assignment:

1) Perform Data sheet of I3, I5, I7 processor
b) Compare Pentium 1, 2, 3, 4 processor
(2) Differentiate b/w Virtual & Cachememory.
(b) Explain the Concept of Virtual memory with the help of Diagram.
(3) Define interrupts why priority is required and how it is restore
b) Explain the Sequence that take place when an Interrupt occur.
(4) As the following memory unit determine no of Address line, I/O lines and no of bytes.

① 64K x 8 ② 16M x 32 ③ 4G x 16 ④ 2K x 16

Instruction set of 8085 :- ① Data transfer group :- MOV Instruction can be done either can with the help of Register or memory

MOV A, R/M → (B, C, D, E, H, L)

1) from Register to Register → MOV A, R
2) Register to Memory → MOV M, R
3) Memory to Register → MOV R, M
4) Immediate Data transfering MVI A, 8 bit
   MVI M, 8 bit

① MOV A, R :- Content of register (B, C, D, E, H, L) are copied to the contents of accumulator MOV related with copy contents
It means after execution of this instruction register R will have same 8 bit data as that of accumulator data. This mode stored in register addressing mode. No flag will affected

② MOV M, R :- This instruction copy the content of register to memory (whose address is specified by HL pair, Register indirect mode, No flag will affected

③ MOV R, M :- Copy the content of memory to register

④ MVI A, 8 bit data :- This instruction copy 8 bit data into accumulator and result is store in ~~register~~ accumulator.

MVI M, 8 bit data :- 8 bit data directly copied into 8 bit memory

Store Instruction :- Store related with transferring of data

① STA , 16 bit Address
② SHLD , 16 bit Address.
③ STAX , rp

1) ~~Flag STA 16 bit Address :- Contents~~

Addressing mode flag dir activation accumulator Contents will transfer to 16 bit address.
No flag is activate

2) SHLD , 16 bit address :- No flag will eff. , Direct register.
Content of HL pair transfered to given 16 bit address

3) STAX , rp :- Indirect , No flag
Content of accumulator transfered to given Register pair (B-C, D-E, H-L)

4) Load instruction :- These instruction are opposite to Store instruction.

① LDA 16 bit Address :- Addressing mode → No flags
Contents of given 16 bit address are transfered to accumulator
Result store in Accumulator.

② LHLD 16 bit address :- Content of 16 bit address are transfered to H-L pair and Result is also stored in H-L pair

③ LDAX rp :- Contents of Register transffered to accumulator.

④ LXI H, 16 bit Data (Exaptional) :- 16 bit data is transfered to H-L pair and H-L pair in this instruction act as a memory pointer.

Exchange instruction :-

① XCHG, rp
② XTHL

① XCHG rp :- This instruction will exchange the contents of register pair (B-C & D-E) with the Content of H-L pair.
Exchang related with Swaping of Content not transfering as well as Copied of Content

② XTHL :- Exchange the Content of H-L pair with Stack pointer.

③ STHL instruction :- This instruction will transferred the Content of H-L to Stack pointer

Airthemetic instruction :-

① ADD R/M } - without Carry
② ADI 8 bit da }

③ ADC R/M } with Carry
④ ACI 8 bit data }

(1) ADD R/M :-

addressing mode	flag	instruction
(1) Register addressing mode		Content of Register/Memory will be added with Content of accumulator & data Stored in accumulator

(2) ADI 8 bit data :- 8 bit data immediately added to accumulator with this instruction and the result is stored in accumulator.

(3) ADC R/M :- Content of Register / Memory are added with accumulator through Carry. It means Carry bit will also be added to accumulator either Set or reset.

(4) ACI 8 bit data :- 8 bit data immediately added with accumulator through carry

Substraction :- In Substraction if accumulator data is less than either register or memory or 8 bit data occurs borrow will generate. Borrow is nothing but again activation of Carry flag.

(1) SUB R/M
(2) SUI 8 bit data
(3) SBB R/M
(4) SBI 8 bit data,

(1) SUB R/M :-

Addressing Mode	Flag	instruction.
Register Addressing mode	*	A

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During substraction 3 condition will lies

(1) If A > R/M | 8 bit data

(2) Of carry flag both will reset

(3) If a = R/M | 8 bit data zero flag will reset

(3) If A < R/M | 8 bit data carry flag will set

Contents of R/M will be substract from accumulator and flags will effects depending upon above 3 condition and result is stored in accumulator.

(2) SUI 8 bit data : 8 bit content will immediately Substracted with content of accumulator and flag will effect depending upon above condition.

(2) SBB R/M : content of R/M will substracted from accumulator through carry (Borrow is nothing i.e is carry)

(4) SBI 8 bit data : 8 bit content of R/M will immediately Substracted from A through carry (Borrow)

Que(1) Substract two no - 15 - 20 using 1's complement & 2's complement

(2) -19(-4) using 1's & 2's complement

(3) design logical gate which will perform all operation NAND, NOR, NOT

Logical Instruction / operation :-
AND, OR, XOR, NOT (Complement operation),
Shifting operation

① AND :- Instruction is ANA R/M
ANI 8bit data
Register addressing mode

ANA R/M :- This instruction perform logical AND operation with the contents of register or memory using accumulator contents and result is store in accumulator
No flag will affe activate

ANI 8bit data :- 8 bit data immediately ~~ene~~ ANDED with contents of accumulator and result is stored in accumulator

② OR :- ① ORA R/M
② ORI 8bit

ORA R/M :- R/M Content Contain are logically OR with contents of accumulator and result stored in accumulator

ORI 8bit :- 8bit data immediately or with contents of accumulator and result is stored in accumulator.

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③ XOR :- ① XRA R/M
XRI 8bit

XRA R/M :- R/M content logically XOR with content of accumulator and result is stored in accumulator & Zero flag will effect

XRI 8bit :- 8bit data immediately XOR with contents of accumulator and result is stored in ⇌ accumulator.

④ NOT :- This operation related with single register here execution as well as storing of result takes places
CMA :- compliment the content of accumulator and result is stored in accumulator
Address mode → Implicit addressing mode
Zero flag will effect.

⑤ Shifting operation :- Shifting will be done with the help of register →. Register is a collection of flipflops.
Shifting is a rotation → Accumulator.
↳ Left shift } without carry
Right shift } Right with carry.

① RRC } → without carry
② RLC } Implicit addressing mode

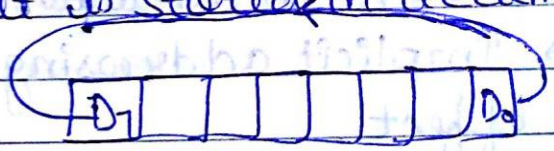
① RAR } - with carry
② RAL }

RRC:- This instruction perform right shift operation using this instruction accumulator content will be shifted right by 1 bit without carry

Register Right Shift

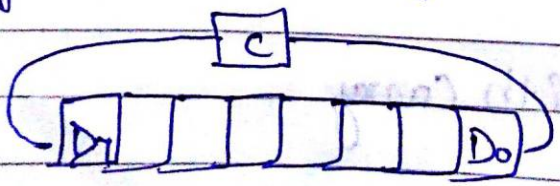
After execution D0 bit position will shift to D7 bit operation.
No flag will affected.

RLC:- Rotate left without carry. This instruction perform left shift operation after execution D7 bit position shifted to D0 bit position and result is stored in accumulator.



Register Left Shift

RAR:- Rotate Right through Carry. This instruction perform right shift operation after execution D0 bit position is shifted to carry flag and carry flag bit position is shifted to D7 bit position
Implicit addressing mode
Carry and zero flag will affected



RAL :- Rotate Left without Carry. This instruction perform left Shift operation through Carry after execution D_7 bit position is shifted to Carry flag and Carry flag bit position is shifted to D_0 bit position
Zero & Carry flag will affect.

Compare operation :- R/M/8 bit
CMP R/M
CPI 8 bit data

① CMP R/M :- This instruction perform compare operation after execution contents of register or memory is compared with the contents of accumulator and flags will affect depending upon the following condition
① If accumulator content less than the R/M/8 bit the Carry flag will activate

② If A = R/M/8 bit then 0 flag will affect.

③ A > R/M/8 bit then 0 & Carry both will reset

Difference between Comparision and substraction:
In Substraction After execution result is stored in accumulator. But in comparision only comparision is done b/w accumulator and R/M/8 bit data ~~it Storage~~ storing will never occur

Reset

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Set and Reset(clear) condition :-

1. STC
2. CLC

1. STC :- Set Carry flag.
2. CLC :- clear Carry flag