Set and Reset(clear) condition :-

① STC
② CLC

① STC :- Set carry flag.
② CLC :- clear carry flag

Branch Control Instruction :-

- Jump
- Subroutine instruction
- Interrupts

Jump are of two type

1) Conditional jump.
2) unconditional jump :- No need of Instruction

JMP 16 bit address

As execution program sequence transffered to even 16 bit address. But without condition condition related with activation and diactivation of flags.

1) Conditional jump :-

- JC 16 bit address Status → CY = 1

JNC " CY = 0

JZ " Z = 1

JNZ " Z = 0

JP " S = 0

JM	16bit address	S=1
JPE	"	P=1
JPO	"	P=0

Statements related with Subroutine :- Call and return are two instruction comes under subroutine program. Call will call the subroutine and return will be used at the end of subroutine to come back to main program.

→ CALL :- CALL are of two type
Condition ~~and~~
Unconditional.

Unconditional :-
CALL 16bit Address :- After execution program sequence is transffered to given 16bit address this address is ~~gene~~ related to address of subroutine. Subroutine is a program which is used again and again in the main program for eg generating delays

Conditional Call :-

• CC	16 bit address	status-CY=1
CNC	16 bit adress	CY=0
CZ	"	Z=1
CNZ	"	Z=0
CP	"	S=0
CM	"	S=1
CPE	"	P=1
CPO	"	P=0

1) Return :- Two type

1) Conditional
   Unconditional

Unconditional

- RET 16 bit Address :- After execution program Sequence is transfer to main program

Conditional Return :-

• RC	16 bit address	Status → CY=1
RNC	"	CY=0
RZ	"	Z=1
RNZ	"	Z=0
RP	"	S=0
RM	"	S=1
RPE	"	P=1
RPO	"	P=0

Interrupts :- 8085 having 5 hardware interrupt
8085 having 8 Software interrupt

RST 0 → 0000H
RST 1 → +8 → 0008H.
RST 2 → 0010H
RST 3 → 0018H
RST 4 → 0020H
RST 5 → 0028H
RST 6 → 0030H
RST 7 → 0038H.

Software interrupt are used to interrupt main program and transffered to Standard address location define by each Software interrupt

Machine and Input/output controlled instruction :-

1) IN Port Address :- After execution contents occur in ports transfer to accumulator
8 bit

2) OUT Port address :- After execution accumulator Content transfer to 8 bit port

Machine Control Instruction :-

① NOP → No operation :- After execution program will Stop for a moment This instruction is used to provide dealy of few microsecond and after execution next instruction of main program will Start executed

② HLT :- Halt will stop the program No instruction will execute after halt.

③ DI → Disable interrupt :- This instruction will disable all interrupt except trap because trap is a non maskable interrupt

④ EI :- Enable Interrup :- will enable all intersupt all flag will be affected.

Page No. Passion
Date

Timing Diagram of 8085 :- It is defined as the display of information during transffering of data reading operation, writing operation, I/P output read operation and input output write operation. Also define as no of Clock or T-States required for the execution of an instruction.

Any instruction can maximum having five machine cycles

Machine Cycle :- It is defined as the operation operated on an instruction. ~~Five~~

Five operation are performed for execution of an instruction depending upon its types

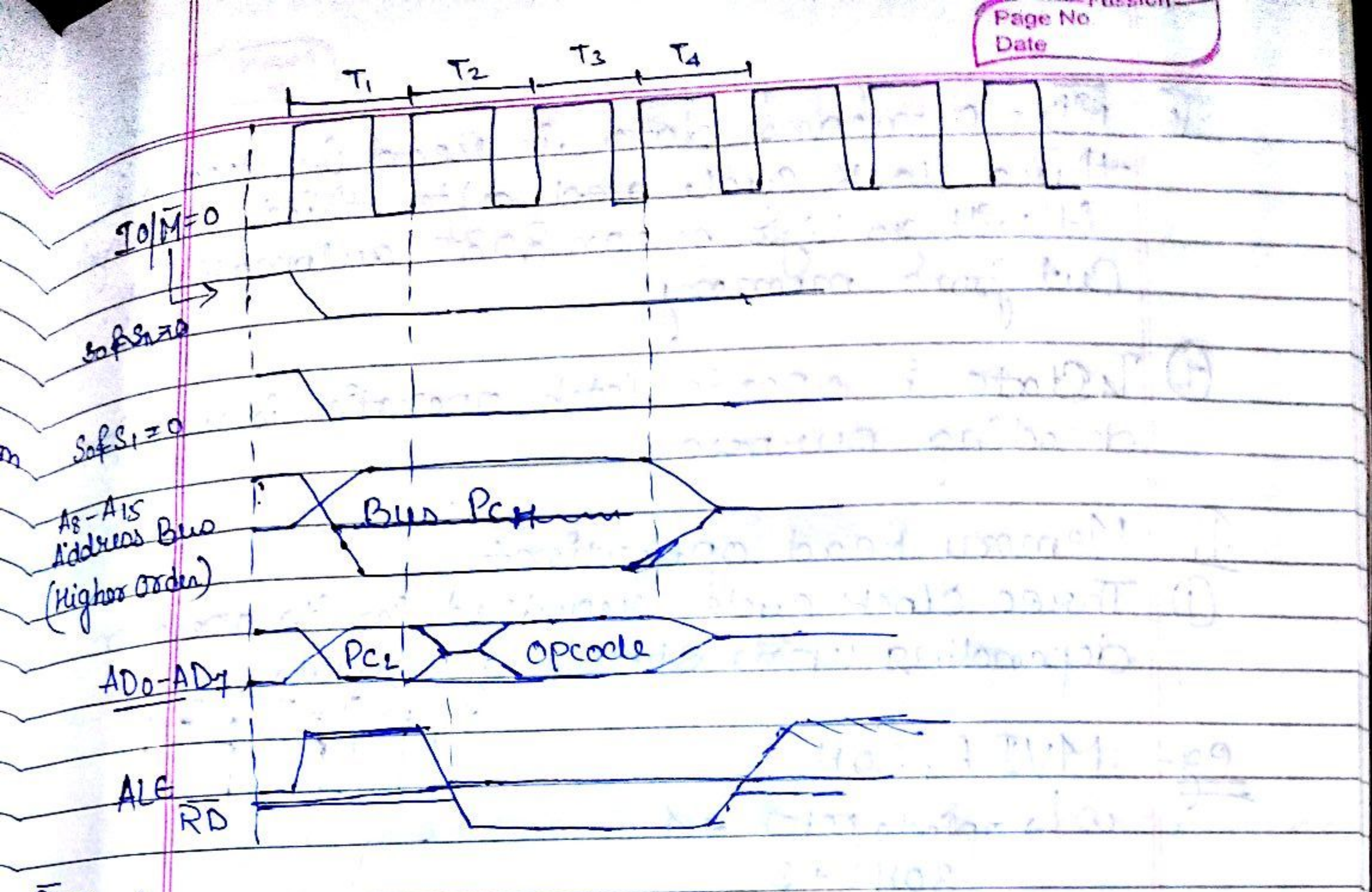
1. Opcode fetch operation
2. Memory read operation
3. Memory write operation
4. I/P O/P read operation
5. I/P O/P write operation

1. Opcode fetch operation :- 4 clock cycle or 6 clock cycle (T-state) required for fetch operation depending upon Status Signal. (So, S, IO/M, ALE)

eg:- MOV A, B → Value in Hexadecimal

↓

1 byte instruction



(1) This instruction related with opcode fetch instruction
(2) Hexcode of this instruction is given which is read from memory to IO/M̄ = 0
(3) Because this is fetch operation S0 = S1 = 0
(4) Higher order address will be send to first three clock cycle.
(5) Low order address / Databus dependent upon ALE signal. When ALE = 1 Address will be sent and ALE = 0 Data will be Sent. First clock Cycle send address and second & third clock Cycle will send data b/w these three Clock Cycle some space is unspecified which is related with Address Latching (Temporarily Storing of Address.

(6) $\overline{RD} = 0$ means data is read in second third clock cycle ~~and~~ after third clock cycle it will go high mean 8085 automatically out from memory.

(7) T_4 State in opcode fetch operation is used for decoding purpose.

II Memory Read operation :-

(1) Three clock cycle required for its operation depending upon status of signals.

eg :- MVI A, 30H

↳ opcode fetch → 4.

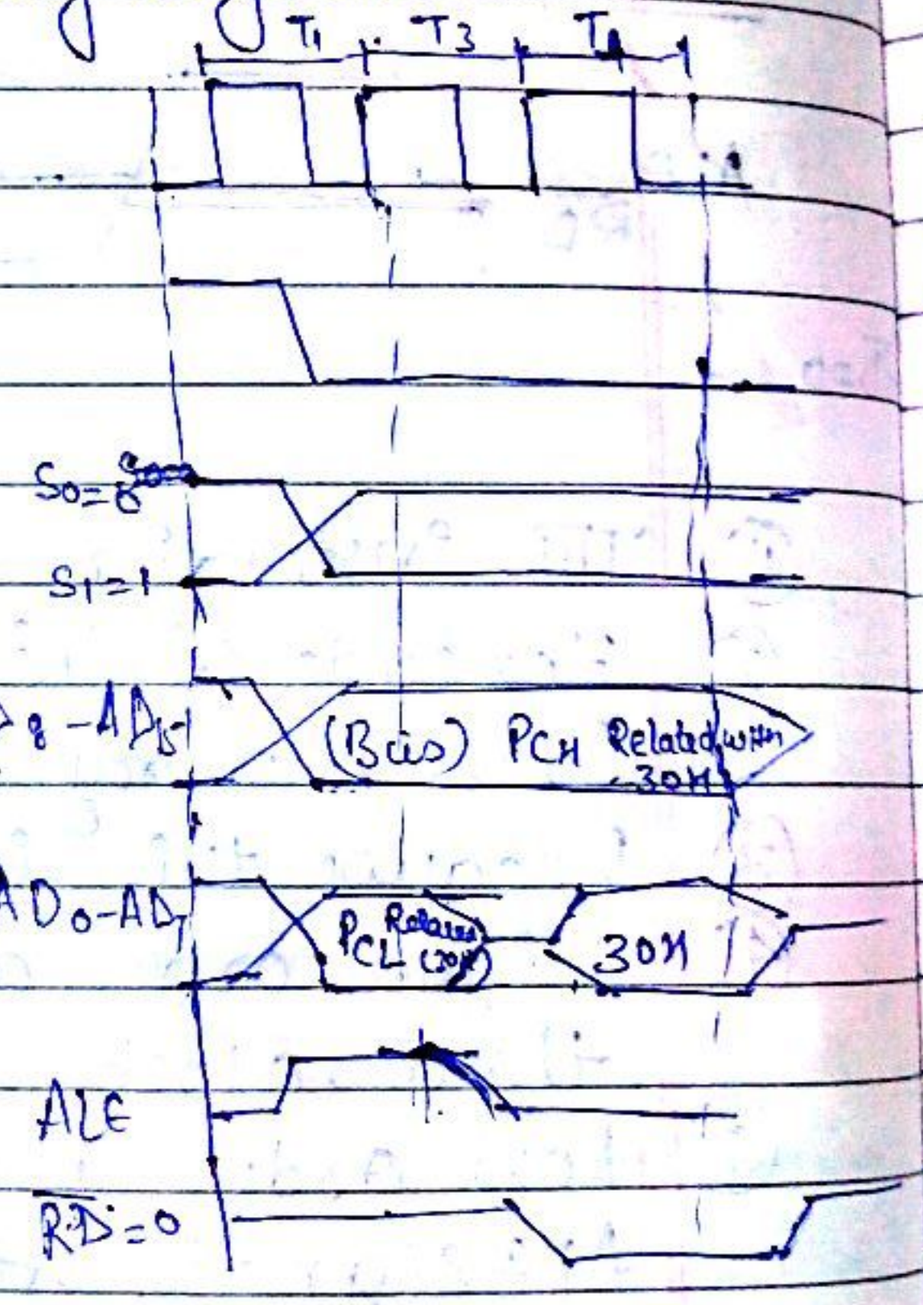
30H + 3

7 T State

f = 3.67 MHz.

Clock cycle T = $\frac{1}{3.67 MHz}$

7 T State = $7 \times \frac{1}{3.67 MHz}$



III Memory write operation :-

eg store operation.

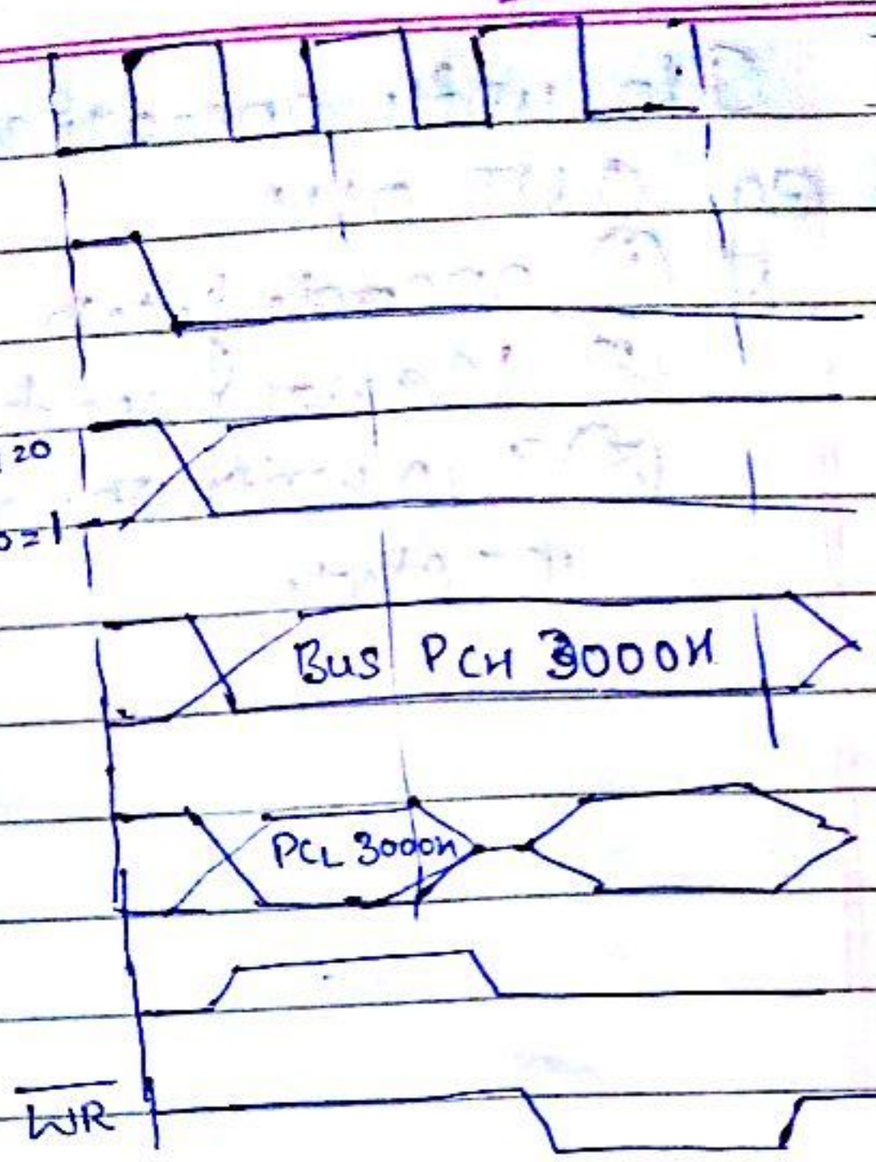
STA 3000H

1) opcode fetch 4

(2) 00 → Memory Read 3

(3) 30 - Memory Read 3

④ Memory Write 3
13 State.



(iii.) I/P O/P read operation :- 3 clock cycle are required.

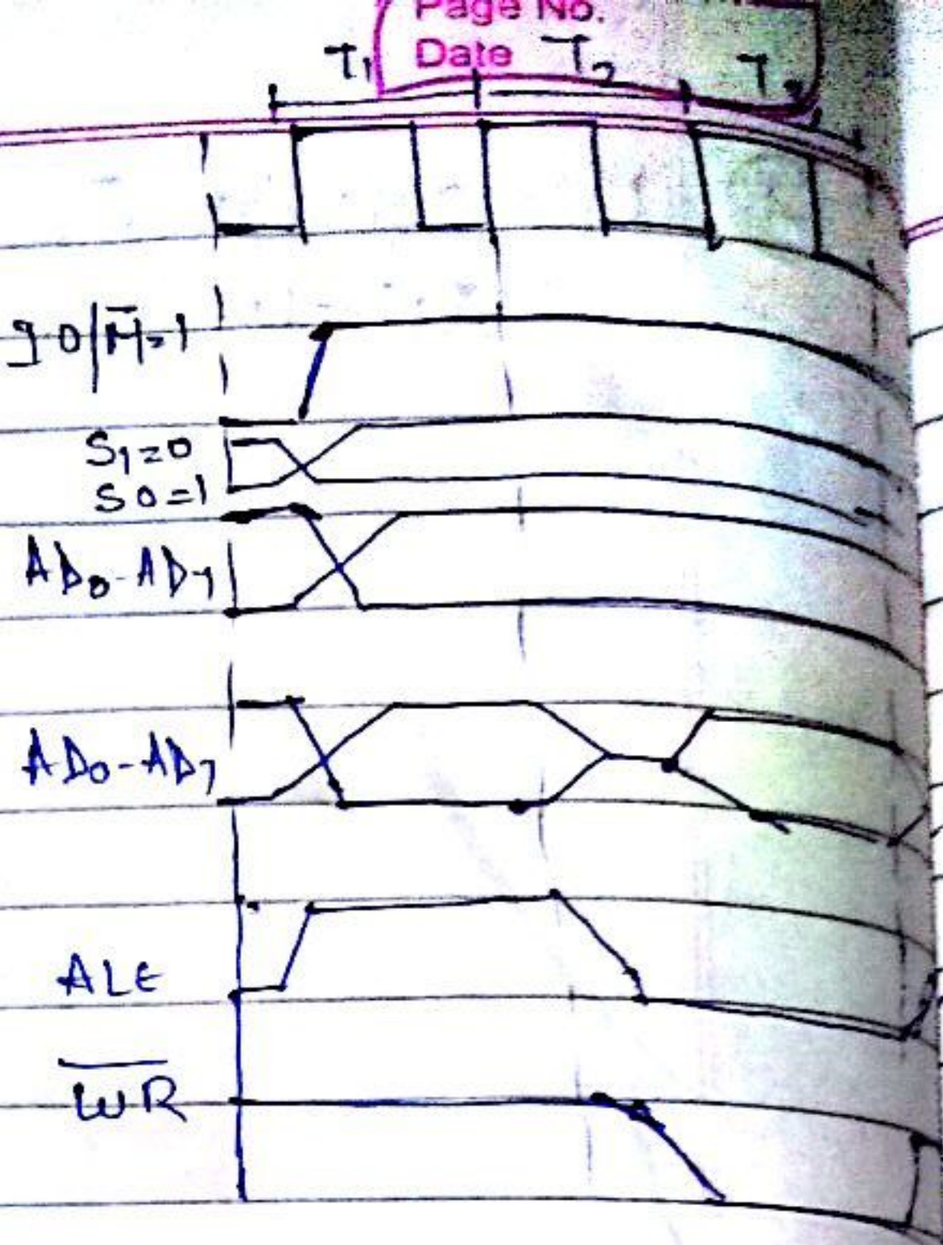
eg IN 01H
↳① opcode fetch 4
② Memory Read 3
③ I/P O/P read operation 3
10T State

IV I/O write operation.

eg OUT 01H

① opcode fetch 4
② Memory read 3
③ I/O write operation 3

10T State



Q ~~HA~~ Write a subroutine for generating ~~delay~~ delay in ~~to~~ main program?

Sol

```
MVI B, ffH
. DCR B
  JNZ  loop
  RET
```

for Subroutine

for normal delay → HLT instead of RET

It is define as transffering of data between microprocessor and memory as well as b/w microprocess & input output devices

Two ways of transffering

① Memory Mapped input output scheme
② I/O mapp I/P, O/P Scheme

① In this scheme single Address space is assigned for both Memory and input output device

It mean address that is assigned for Memory location can neva be assigned to input output device Both having different address.
In this scheme input output device act as a memory location
This scheme is applied for small Data transffering

I|O map I|P O|P scheme:- In this scheme both devices have assign same address. The scheme is related with 80 85 microprocessor. In which IO|$\overline{M}$ is the pin which define either address is of memory location or input output device.
IO|$\overline{M}$ = 0 mean address define assigned for memory location
IO|$\overline{M}$ = 1 mean address assigned for input output device

- Two more instruction used in this Scheme are in and OUT

IN related with reading of data form input output devica.
OUT relate transffering of data form accumulator to input output accumulator

Another mode of data transfering is done by DMA, data transfer technique / Scheme

↳ Direct Memory Access

HOLD pin is used for peripherial devices by taking its request and second pin related with $\overline{HLDA}$

Page No.
Date

Two Scheme used for DMA Data Controlling machine

① Cyclic Stealing :- It is related with byte by byte
② Burst Mode of data transfer :- All the data transfer together